

## CLAIMS

1           1. A programmable interface comprising:  
2           a register file having registers, each register having a type;  
3           a run control register;  
4           a microcontroller bidirectionally communicates with the register file and the run  
5 control register;  
6           a Code Store SRAM, bidirectionally communicating with the microcontroller; and  
7           executable code, loaded onto the Code Store RAM;  
8           wherein the Code Store SRAM and the run control register bidirectionally  
9 communicates with a system processor.

1           2. A device, as defined in claim 1, the types of the registers are selected from a  
2 group that includes timer, General purpose, external I/O, internal I/O, shared, and  
3 interrupt.

1           3. A device, as defined in claim 2, when one of the registers has a type of  
2 external I/O, the register including edge detect logic.

1           4. A device, as defined in claim 2, wherein the register type further includes  
2 FIFO registers, operative to communicate with a direct memory access controller.

1           5. A device, as defined in claim 3, the executable code implements a laser printer  
2 mechanism communications interface and a vertical top-of-page synchronization  
3 interface.

1           6. A device, as defined in claim 1, wherein the executable code is selected from a  
2 group that includes serial interfaces, parallel interfaces, serial peripheral interface (SPI),  
3 Synchronous Serial Interface (SSI), MicroWire, Inter Integrated Circuit (I2C), control  
4 area network (CAN), UART, IEEE1284, LCD interface, front panel interface, and  
5 MODEM.

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